



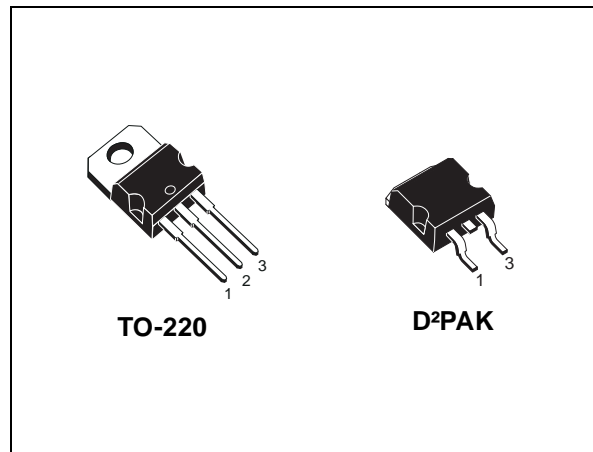
# STB8NM60D STP8NM60D

N-CHANNEL 600V - 0.9Ω - 8A - TO-220/D<sup>2</sup>PAK  
Fast Diode MDmesh™ Power MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>TOT</sub>
STB8NM60D	600V	< 1.0Ω	8A	100W
STP8NM60D	600V	< 1.0Ω	8A	100W

- High dv/dt and avalanche capabilities
- 100% avalanche rated
- Low input capacitance and gate charge
- Low gate input resistance
- Fast internal recovery diode



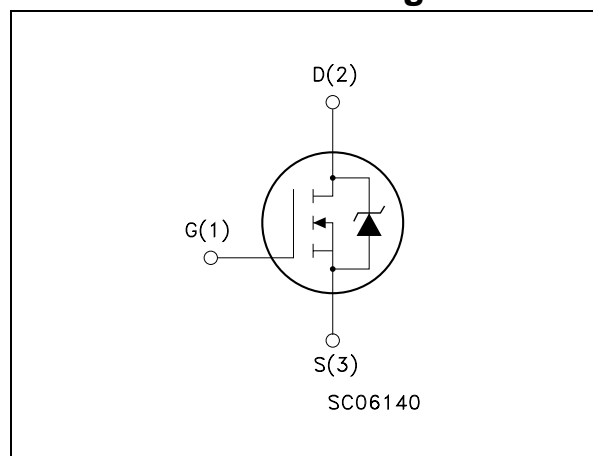
## Description

The FDmesh™ associates all advantages of reduced on-resistance and fast switching with an intrinsic fast-recovery body diode. It is therefore strongly recommended for bridge topologies, in particular ZVS phase-shift converters

## Applications

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

## Internal schematic diagram



## Order codes

Sales Type	Marking	Package	Packaging
STB8NM60D	B8NM60D	D <sup>2</sup> PAK	TAPE & REEL
STP8NM60D	P8NM60D	TO-220	TUBE

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-Source Voltage ( $V_{GS} = 0$ )	600	V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20k\Omega$ )	600	V
$V_{GS}$	Gate-Source Voltage	$\pm 30$	V
$I_D$	Drain Current (continuous) at $T_C = 25^\circ C$	8	A
$I_D$	Drain Current (continuous) at $T_C = 100^\circ C$	5	A
$I_{DM}^{(1)}$	Drain Current (pulsed)	32	A
$P_{TOT}$	Total Dissipation at $T_C = 25^\circ C$	100	W
	Derating Factor	0.8	W/ $^\circ C$
$dv/dt^{(2)}$	Peak Diode Recovery voltage slope	20	V/ns
$T_J$ $T_{stg}$	Operating Junction Temperature Storage Temperature	-65 to 150	$^\circ C$

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 5A$ ,  $di/dt \leq 400A/\mu s$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	1.25	$^\circ C/W$
$R_{thj-amb}$	Thermal resistance junction-ambient Max	62.5	$^\circ C/W$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ C$

**Table 3. Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	2.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25^\circ C$ , $I_D = I_{AR}$ , $V_{DD} = 50V$ )	200	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu A, V_{GS} = 0$	600			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating},$ $V_{DS} = \text{Max Rating}, T_c = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate Body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 30V, V_{DS} = 0$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	3	4	5	V
$R_{DS(on)}$	Static Drain-Source On Resistance	$V_{GS} = 10V, I_D = 2.5A$		0.9	1	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward Transconductance	$V_{DS} = I_{D(on)} \times R_{DS(on)max}$ $I_D = 2.5A$		2.4		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		380 170 14		pF pF pF
$C_{oss \text{ eq.}}^{(2)}$	Equivalent Output Capacitance	$V_{GS} = 0, V_{DS} = 0V \text{ to } 480V$		60		pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 400V, I_D = 5A$ $V_{GS} = 10V$ (see Figure 13)		15 4 8	18	nC nC nC

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%
2.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=300V, I_D=2.5A,$ $R_G=4.7\Omega, V_{GS}=10V$ (see Figure 12)		13		ns
$t_r$	Rise Time			10		ns
$t_{d(off)}$	Turn-off Delay Time			26		ns
$t_f$	Fall Time			8		ns
$t_{d(off)}$	Turn-off Delay Time	$V_{DD}=480V, I_D=5A,$ $R_G=4.7\Omega, V_{GS}=10V$ (see Figure 12)		8		ns
$t_f$	Fall Time			8		ns
$t_c$	Cross-over Time			14		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				5	A
$I_{SDM}^{(1)}$	Source-drain Current (pulsed)				20	A
$V_{SD}^{(2)}$	Forward on Voltage	$I_{SD}=5A, V_{GS}=0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD}=5A, di/dt = 100A/\mu s,$ $V_{DD}=50 V, T_j=25^\circ C$		107		ns
$Q_{rr}$	Reverse Recovery Charge			330		nC
$I_{RRM}$	Reverse Recovery Current			6		A
$t_{rr}$	Reverse Recovery Time	$I_{SD}=5A, di/dt = 100A/\mu s,$ $V_{DD}=50 V, T_j=150^\circ C$		178		ns
$Q_{rr}$	Reverse Recovery Charge			640		nC
$I_{RRM}$	Reverse Recovery Current			7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

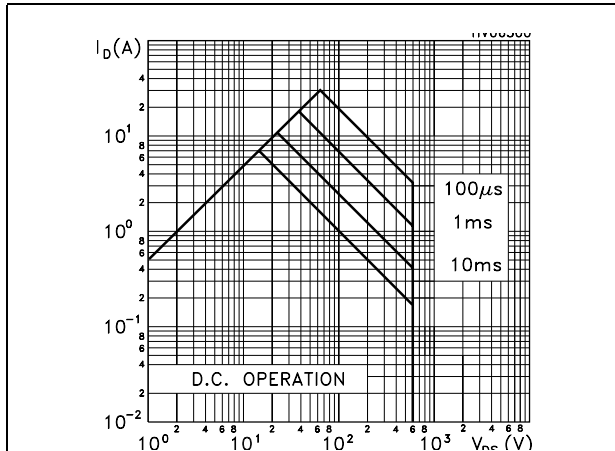


Figure 2. Thermal impedance

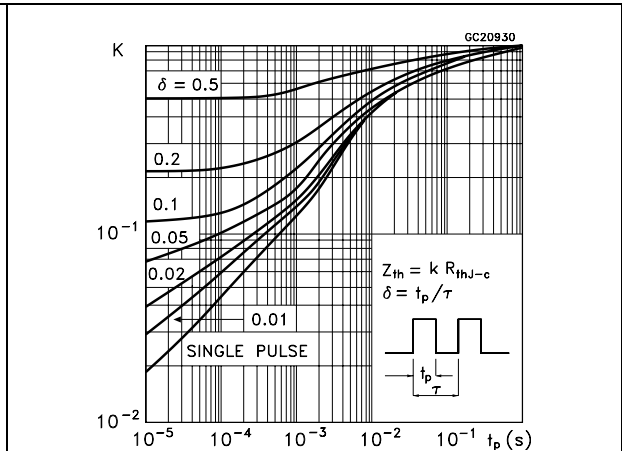


Figure 3. Output characteristics

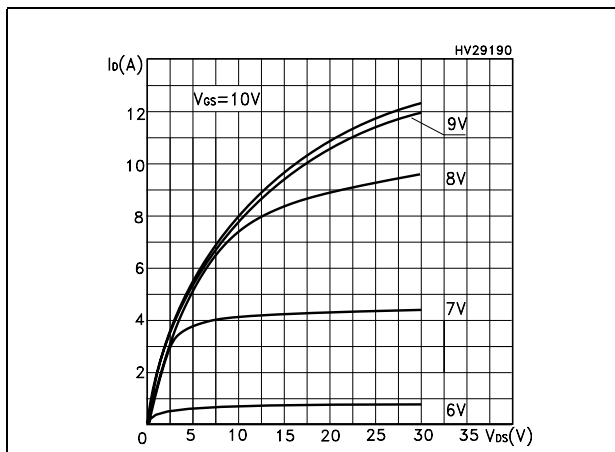


Figure 4. Transfer characteristics

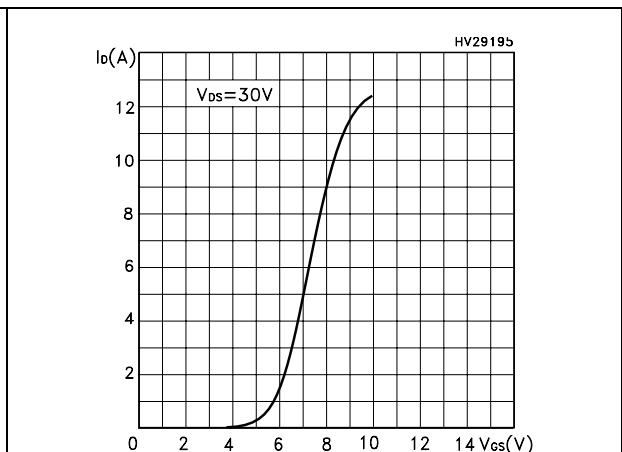


Figure 5. Transconductance

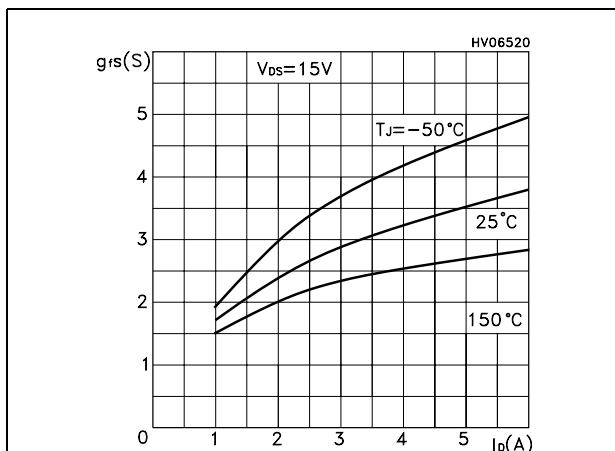


Figure 6. Static drain-source on resistance

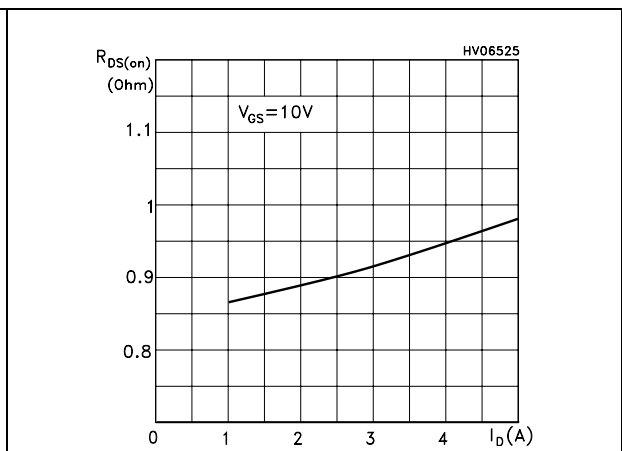


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

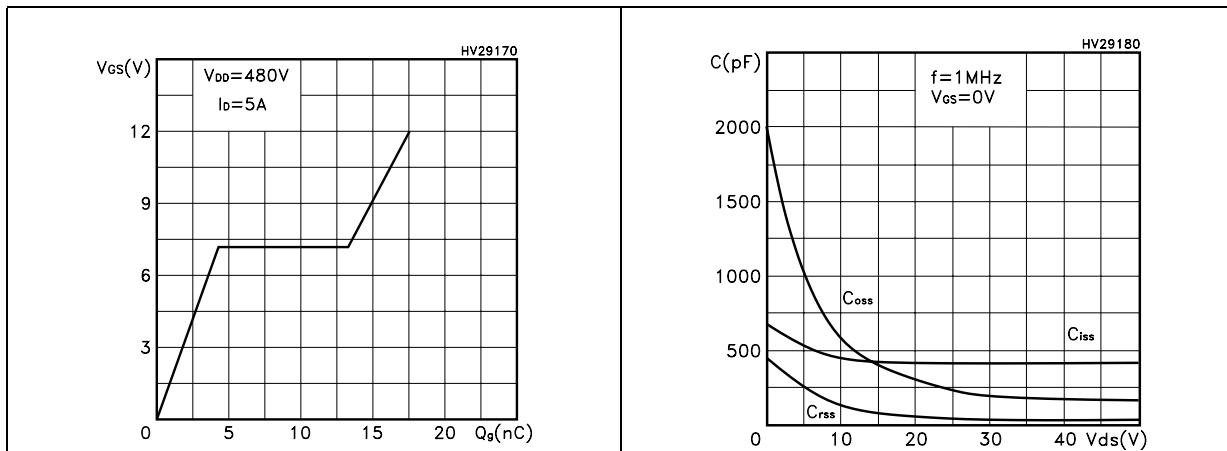


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

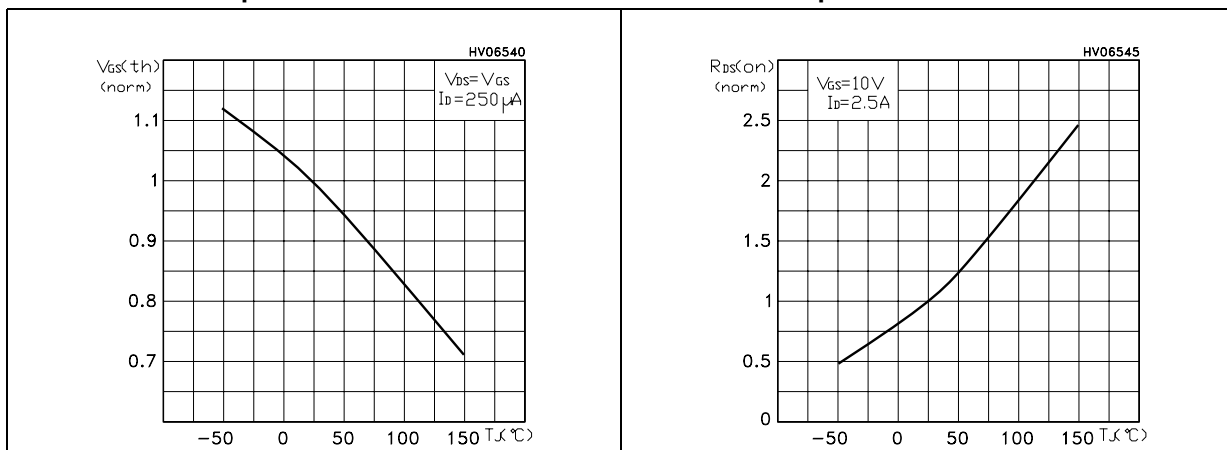
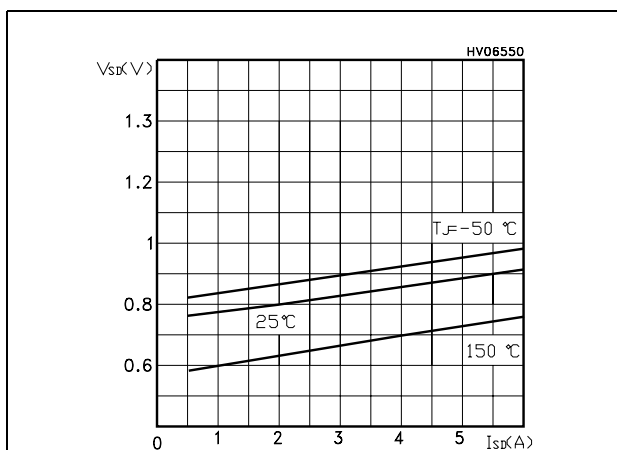


Figure 11. Source-drain diode forward characteristics



### 3 Test circuit

Figure 12. Switching times test circuit for resistive load

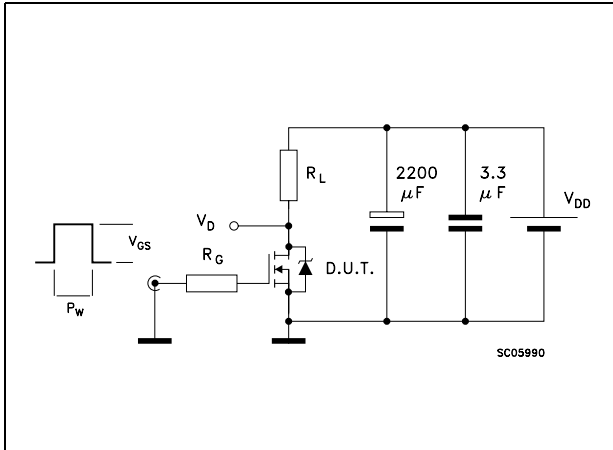


Figure 13. Gate charge test circuit

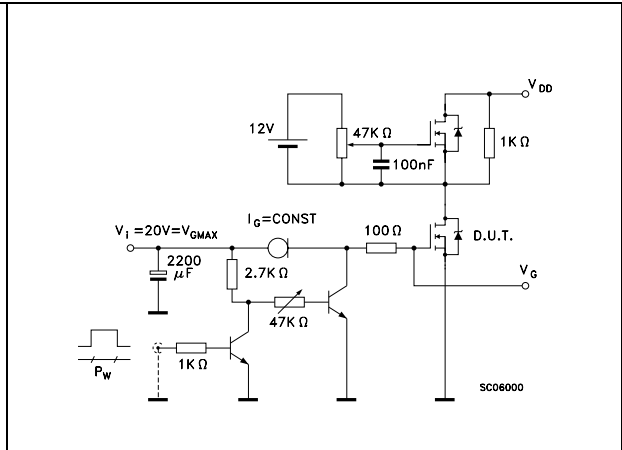


Figure 14. Test circuit for inductive load switching and diode recovery times

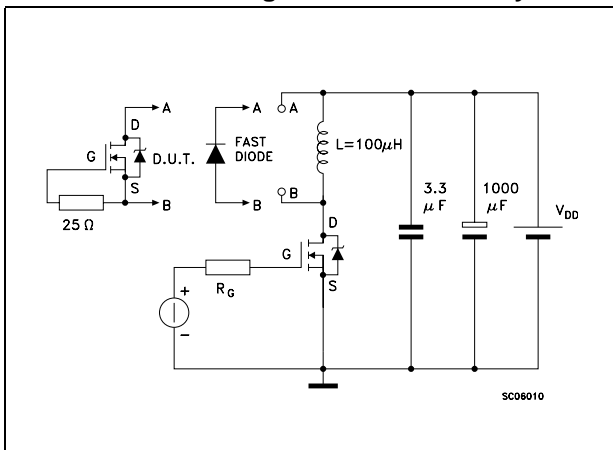


Figure 15. Unclamped Inductive load test circuit

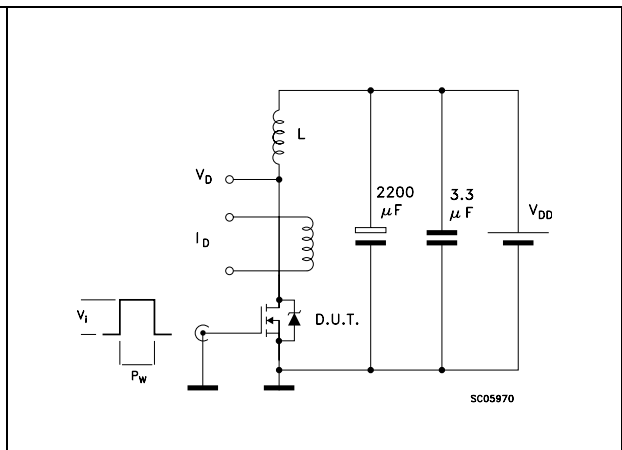


Figure 16. Unclamped inductive waveform

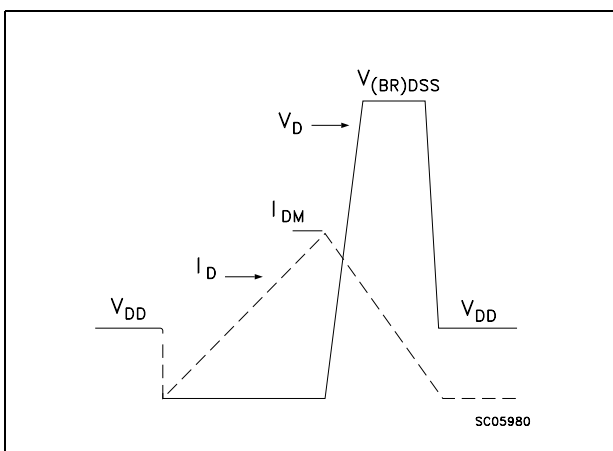
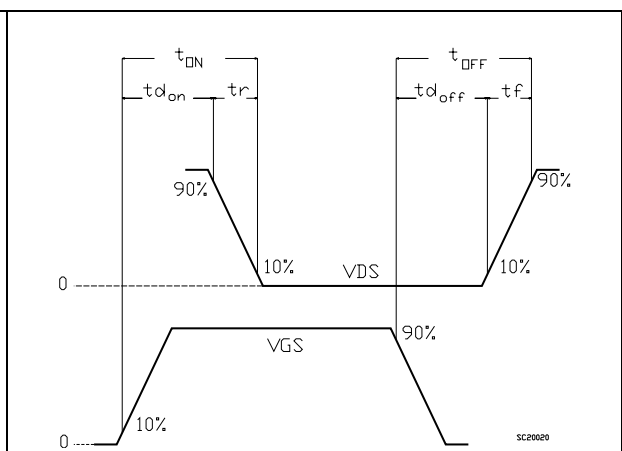


Figure 17. Switching time waveform



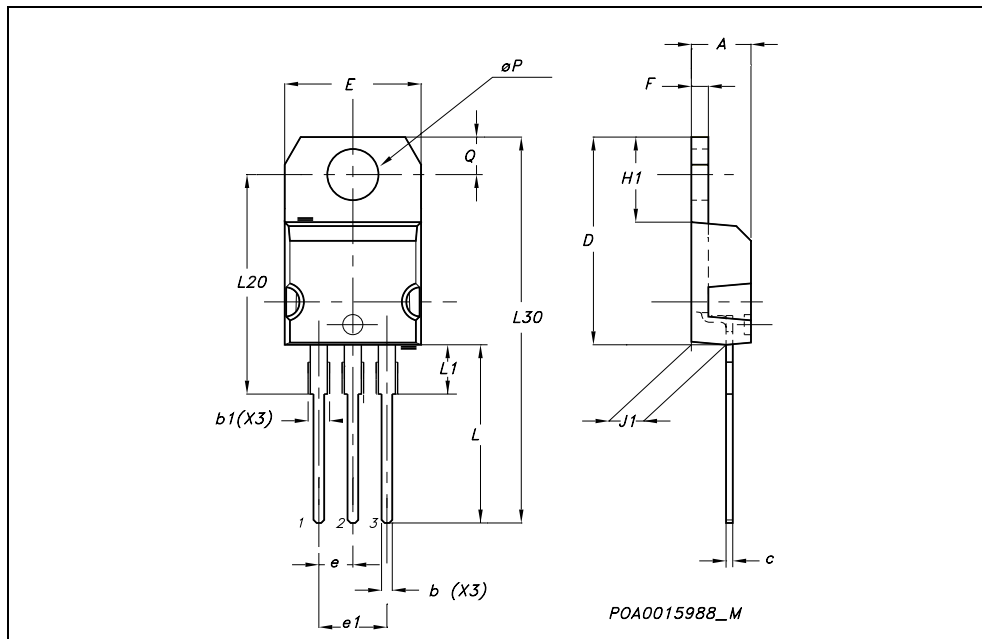
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)



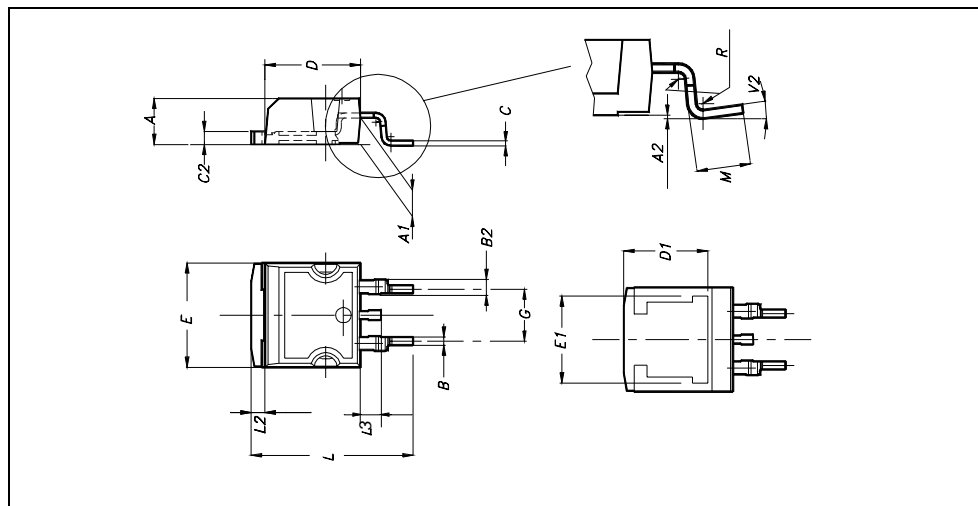
**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



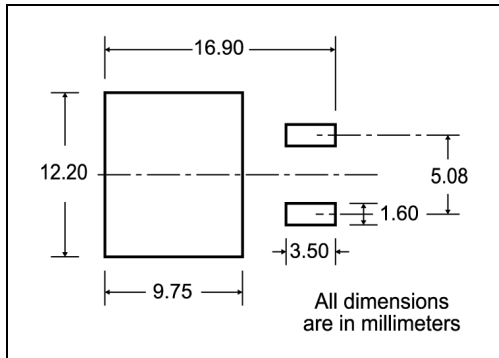
**D<sup>2</sup>PAK MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



# 5 Packaging mechanical data

## D<sup>2</sup>PAK FOOTPRINT



## TAPE AND REEL SHIPMENT

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

\* on sales type

## 6 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
13-Jan-2006	1	Initial release.
15-Feb-2006	2	Modified Description on first page

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